MOS TECHNOLOGY

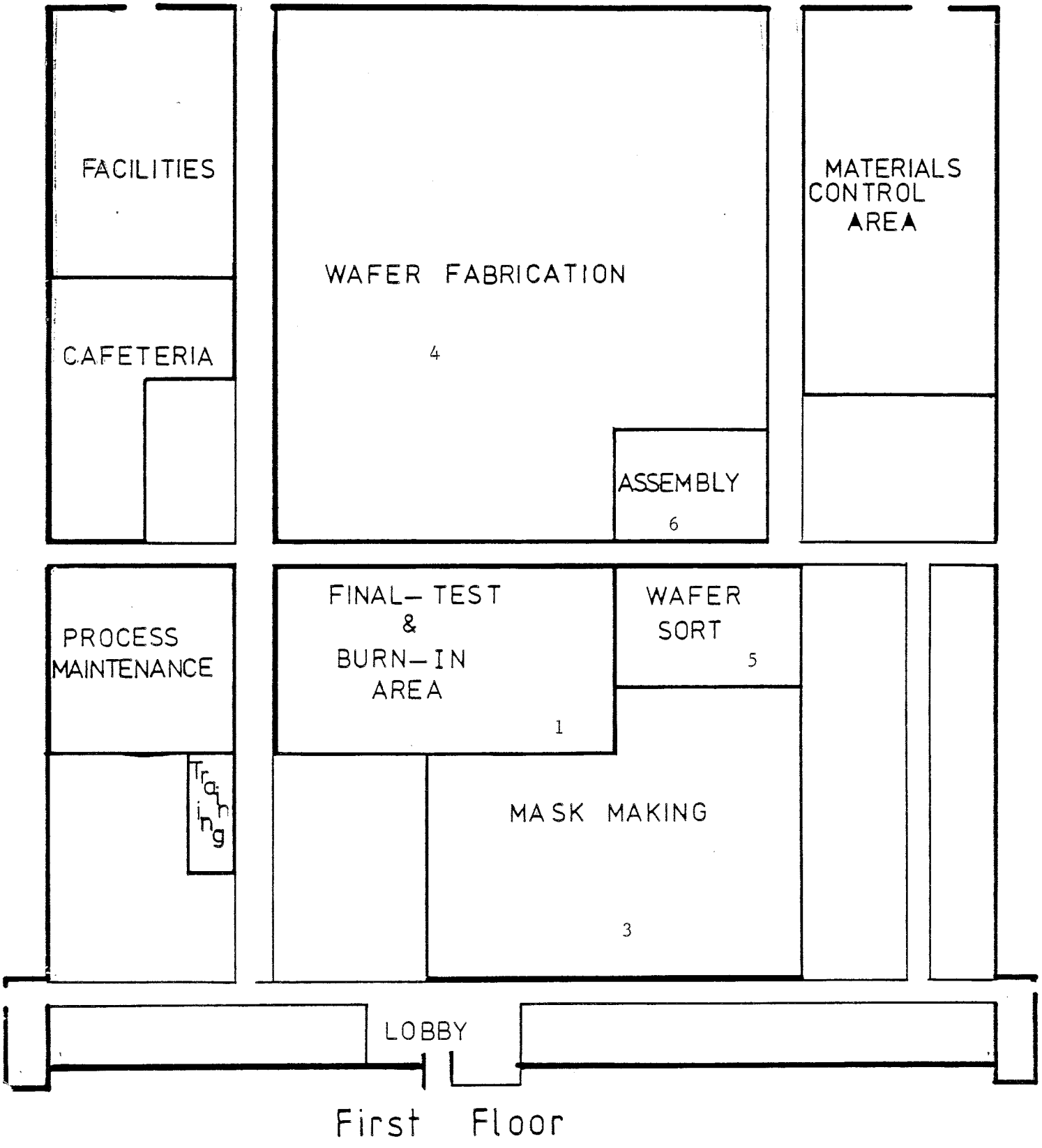
COMMODORE SEMICONDUCTOR GROUP

PLANT TOUR

OCTOBER 6, 1981

GROUP NO: 6

TOUR GUIDE: G. VENKATESH



First Floor

M.O.S. TECHNOLOGY

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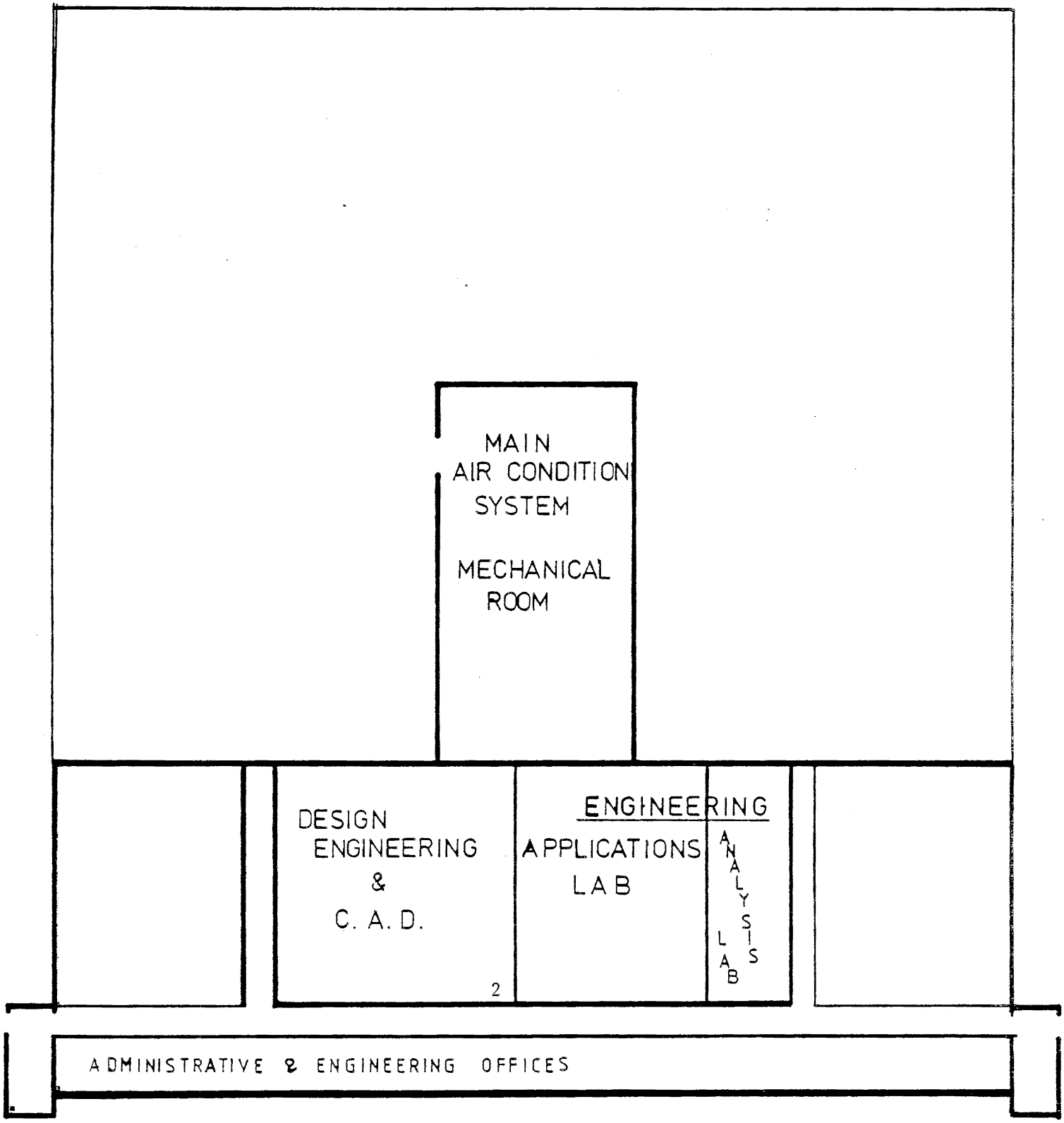


Second Floor

M.O.S. TECHNOLOGY

TABLE OF CONTENTS

PAGE

I. INTRODUCTION. 1

A. Evolution of MOS (Metal Oxide Silicon)
B. Advantages of MOS LSI (Large Scale Integration)

1. Economic
2. Performance

II. DESIGN. 3

III. PHOTOMASK FABRICATION 4

IV. WAFER FABRICATION 6

A. General
B. Process Requirements (Basic)
C. Major Fab Operations
D. Chemical Vapor Deposition
E. Backside Processing

V. WAFER SORT. 10

VI. ASSEMBLY. 12

A. Diamond Saw
B. Plate
C. Die Visual
D. Die Attach
E. Lead Bond
F. Preseal Visual
G. Mold (plastic) and Seal (ceramic)
H. Mark
I. Pack

VII. FINAL TEST. 15

VIII. SUPPORT ACTIVITIES. 16

A. Circuit Design
B. Product Engineering
C. Process Engineering
D. Quality Assurance
E. Equipment Maintenance
F. Facilities Maintenance

EVOLUTION OF MOS LSI

I. INTRODUCTION

This booklet contains a synopsis of the major manufacturing operations of a semiconductor activity. These operations tend to vary from company to company but in general are representative of the industry. To provide some background, the following chronological summary is presented before discussing the manufacturing process.

A. Evolution of MOS LSI (Metal Oxide Silicon)

1930 - Initial attempts to realize active solid-state transistors were undertaken.

1948 - First working model of field-effect transistor (FET) developed at Bell Labs.

1952 - FET with control electrode consisting of reverse - biased junction defined.

1955 - FET's built and tested but fabrication techniques unsuccessful because process unstable; result was poor product yields.

1960 - Major breakthrough in semiconductor processing with development of silicon planar process. Individual MOS transistors produced.

1964 - Simple integrated circuits produced - 30 years after FET concept discovered.

1967 - Major process control problems solved allowing very stable performance characteristics and increased yields, i.e., reduced costs.

1974 - The MOS process demanded high-quality silicon wafers and produced 2 - 3 inch diameter wafers to further reduce manufacturing costs. Typical silicon chips comprised the equivalent of 400 transistors.

1980 - Wafer diameters approaching 4 - 5 inches with silicon chips containing the equivalent of 60,000 transistors.

B. Advantages of MOS LSI (Large Scale Integration)

1. Economic

- Low system maintenance cost to user as a result of high-reliability and low maintenance.
- Reduced system cost to user because of large scale integration, i.e., reduces number of semiconductors to realize system.
- Reduced cost for complex devices and logic arrays.
- Design of MOS arrays is possible to automate with computer program.

2. Performance

- Higher performance systems allowable due to an increase in complexity of circuits without severe cost impact.
- Improved system reliability and maintainability.
- Performance readily predictable as compared to other technologies.

II. DESIGN

The design of a "large scale integrated circuit" can be separated into eight different steps. The process begins with the conception of an idea for a new LSI circuit. Inputs are received from various sources including Marketing and CBM Systems Design. The first step in the process is to define the "architecture." What is the chip supposed to do and how will it do it? Once defined, circuit design begins.

There is very little pencil and paperwork. From the circuit description computer simulations are used to assist in defining the exact circuitry required. When the circuit design is complete, "Layout Specialists" draw to scale how the final circuit will look as a finished product. On a large device that may include 100,000 transistors it is impossible to draw every single element. For example, on a random access memory circuit (RAM) with 64,000 cells, only one cell is actually drawn. From this layout on paper, using a "digitizing station," the scaled drawings are converted to computer "data bases." The data base is edited in a "computer aided design" or "CAD" System. The one cell that was drawn is duplicated to 64,000 cells. At the end of this editing process, the complete circuit description is contained in a new computer data base. The computer also checks to insure that no "design rule" violations were made. This checking process that could take man years is done in a matter of a few hours using the computer. A variety of cells representing many different electrical circuit functions can be designed and stored in the computer for subsequent use in designing circuits for a broad range of applications.

The last step in the process is to convert the data base to magnetic tape which contains the specific information required to generate masks. Masks are used in the wafer fabrication area much as photographic negatives are used in printing photos. Selective exposure is used to define the areas in Silicon to be etched away or chemically altered to form the actual circuit elements.

III. PHOTOMASK FABRICATION

A. General

Photomask Fabrication refers to the manufacture of the photo tool used to produce the MOS circuit. High quality glass is the principal material used in the manufacture of photomasks because of flatness and stability. This glass is coated with a thin film of emulsion or chromium.

B. Process Requirements

Because of the small feature sizes and critical dimensional and alignment tolerances the following requirements are minimum for photomask processing.

- Precise temperature and humidity control.
- High purity deionized water, gases and chemicals.
- High precision, computer controlled photographic equipment.
- HEPA filtered environment.
- Skilled Personnel.

C. Major Maskmaking Operations

The following terms are used in the Photomask area. Photomask is the area in which the circuit design is converted from a magnetic tape to the photographic tool used in the circuit manufacturing process.

Magnetic Tape - Nine track tape, supplied by the CAD department, containing the circuit design in digital format.

Reticle - A single circuit pattern at 10X part size. The reticle is produced photographically on an emulsion coated glass substrate by a very precision, computer controlled camera system.

Photomask - A chromium coated glass substrate containing an array of images of a single circuit pattern. This operation utilizes the reticle as its tool and optically reduces the reticle image 10X to part size and step and repeats an array of circuit patterns on a chromium coated glass substrate.

IV. WAFER FABRICATION

A. General

Wafer fab refers to that part of the factory where diffusion/oxidation, ion implantation, thin film deposition, and photomasking operations take place.

- Silicon is the principal material used for the manufacturing of semiconductors because a dense, uniform oxide can be grown over its surface remaining stable for wide temperature ranges.
- Silicon semiconductor devices are fabricated (fab'ed) on thin crystal substrates called wafers; wafers are sliced from a cylindrical ingot of silicon.

B. Process Requirements (Basic)

Human hair is 1 to 2 mils thick. One mil equals one-thousandth of an inch (25.4 microns). The lines and distances defined in today's semiconductors typically range between four and five microns. As a result, the following requirements are minimum for wafer fabrication.

- Precise control of environmental temperature and humidity.
- Extremely high purity deionized (DI) water, gases and chemicals.
- High precision and control manufacturing equipment which allows reproducibility.
- Precision design of the part to be manufactured.
- Skilled (well-trained) labor and engineering capable of consistently reproducing the hundreds of operations required for circuit manufacturing.

C. Major Fab Operations

The following terms are used in the wafer fab area. Basically, the wafer fab is the area in which the raw silicon wafer is processed into thousands of integrated circuits on the wafer.

Oxidation - The process that causes a layer of oxide to be deposited on the wafer. This is accomplished in "boats" which are loaded into oxidation furnaces.

Diffusion - The process that creates the PN junction developing the transistor effect. In this process a dopant is introduced (typically boron) in a gaseous form and diffused as a result of temperature and time (see figures 1 and 2).

Ion Implantation - This is the introduction of ions (charged particles) to the silicon crystal. The ions are essentially shot into the crystal field by an implanter.

Photomasking - In the production of integrated circuits there can be five to ten masking steps, i.e., areas implanted or diffused, capacitors, resistors and metal interconnects. Each mask will usually carry a pattern repeated hundreds of times. A scratch or smudge on the mask will create a defect on the wafer and render that device useless (see figure 3).

D. Chemical Vapor Deposition

This is the latter step of the fab process and is typically done to increase oxide thickness and to protect the active surface of the wafer against scratches. Some examples are vapox and silicon nitride. The latter, silicon nitride, is also a good barrier against moisture in addition to being scratch resistant. Both processes are primarily used to protect the surface of the finished device.

E. Backside Processing

There are several reasons for processing the backside of the wafer. The key reasons are as follows:

- Removing unwanted transistors (PN junctions). (Refer to figure 1)
- Physically thinning the wafer so the scribed die will fit the cavity of a package.
- Increasing the electrical conductivity of the wafer's backside.

FIGURE 1

P-N JUNCTIONS

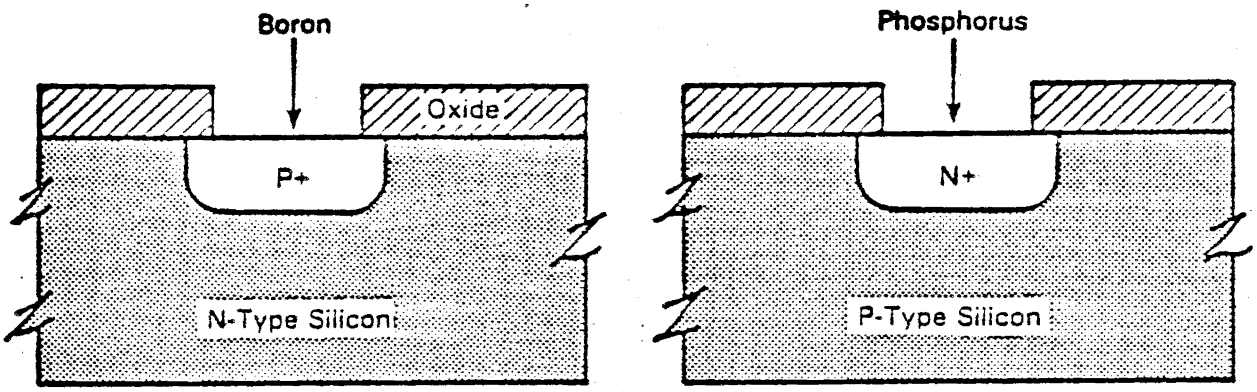


FIGURE 2

CROSS SECTION OF AN N-CHANNEL MOS TRANSISTOR

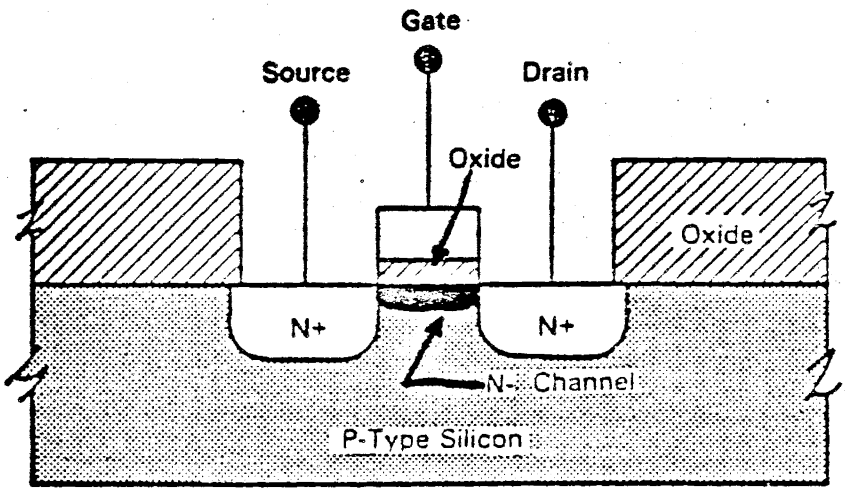
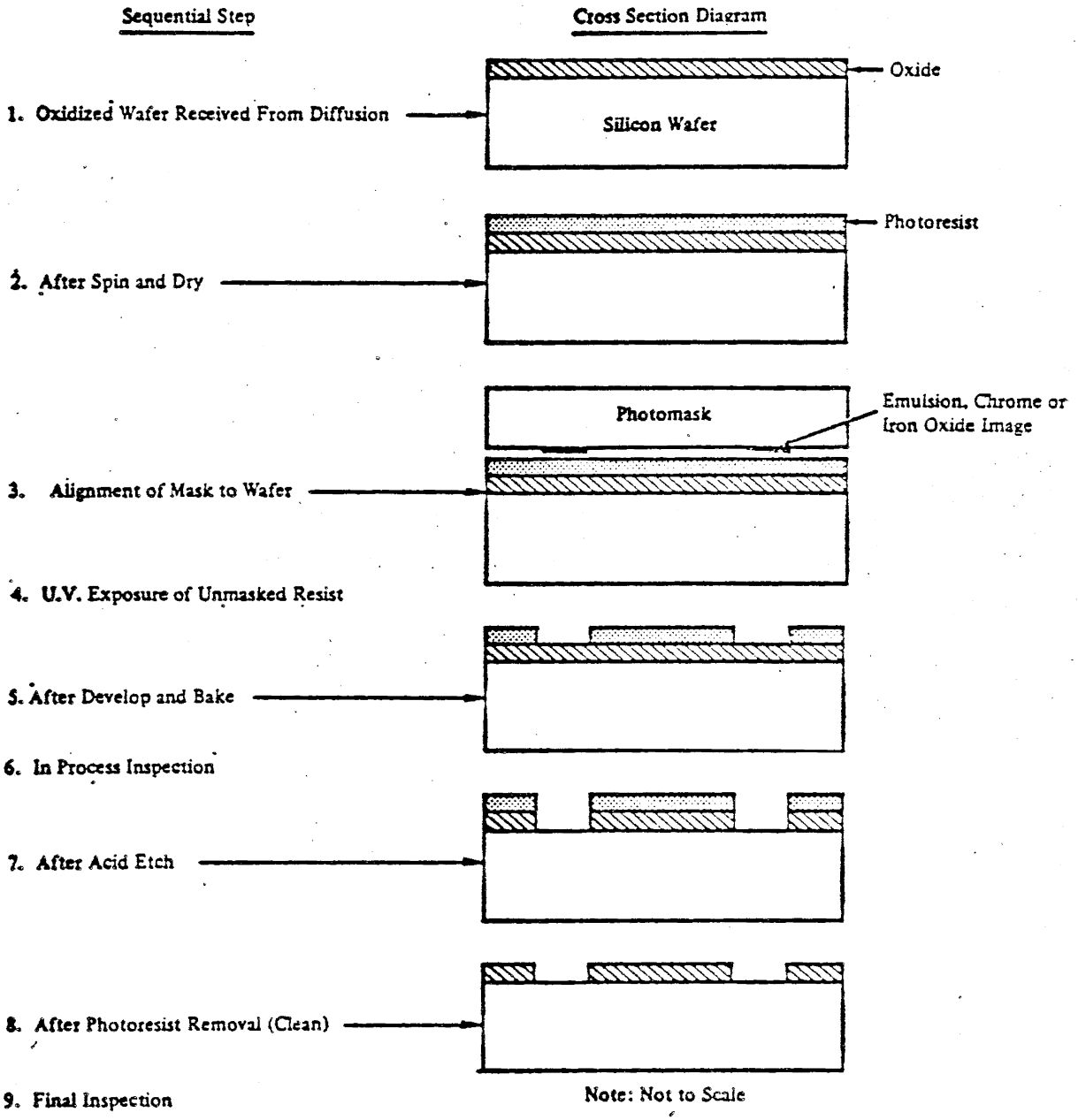


FIGURE 3

PHOTOMASKING PROCESS STEPS

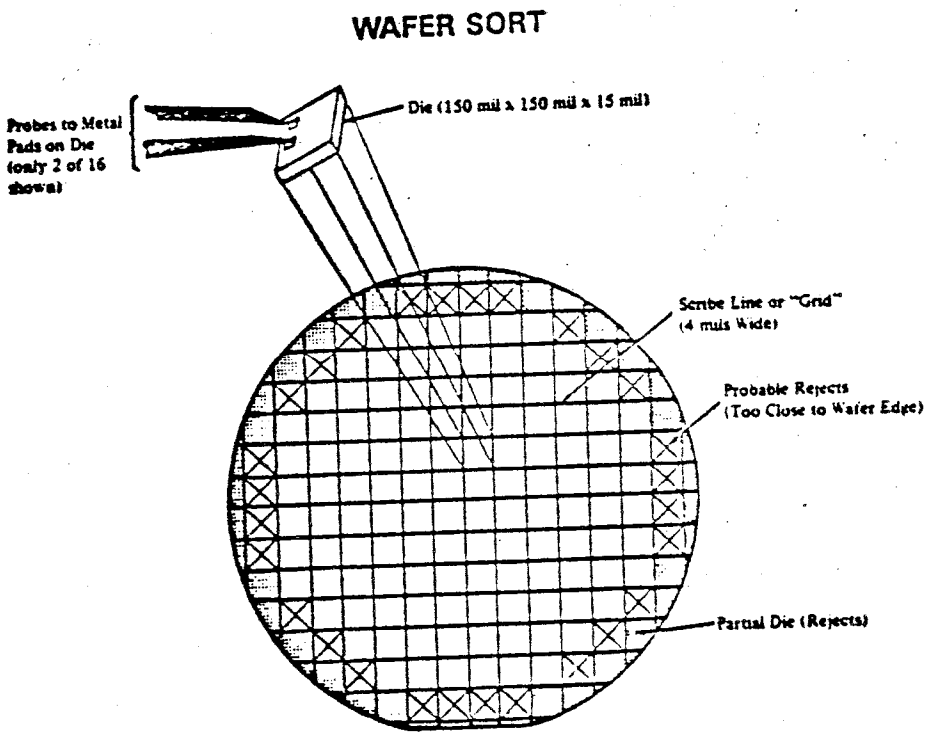


V. WAFER SORT

The Wafer Sort Test is also referred to as wafer probe. A wafer probe machine checks the functionality of each die on the wafer. The machine automatically steps across the wafer checking each die. The following are objectives of wafer sort (see figure 4).

- To reject potentially bad dice (circuits) so that additional costs are not incurred by putting defective circuits into a package. Faulty circuits are marked with a dot of ink.
- Each die is subjected to a test to insure a high percent change of it passing the final test when it reaches that point.
- Feedback information to fab to insure that processing problems are detected and corrected thereby maintaining acceptable product cost.

FIGURE 4


WAFER SORT
Probes to Metal Pads on Die (only 2 of 16 shown)
Die (150 mil x 150 mil x 15 mil)
Scribe Line or "Grid" (4 mils Wide)
Probable Rejects (Too Close to Wafer Edge)
Partial Die (Rejects)

VI. ASSEMBLY

The following major assembly operations are defined:

A. Diamond Saw

Wafers are placed on a machine which automatically cuts through the wafer along grid lines between the circuits. This cut allows the wafer to be separated into individual dice.

B. Plate

An operator separates the good and reject die using a special pick-up tool.

C. Die Visual

The good die are now inspected visually for mechanical defects such as scratches, chip outs, or other large defects.

D. Die Attach

Good dice are mounted in packages and bonded at high temperature with a gold preform.

E. Lead Bond

This step is the actual connection of the terminal points on the die to the corresponding leads on the package.

F. Preseal Visual

This visual inspection screens out any units that may have been damaged during previous assembly steps.

G. Mold (plastic) or Seal (ceramic)

For plastic packaging molten plastic is injected into the mold to form the plastic body. For ceramic packaging the ceramic body is sealed with a metal lid which protects the device from external environmental conditions.

H. Mark

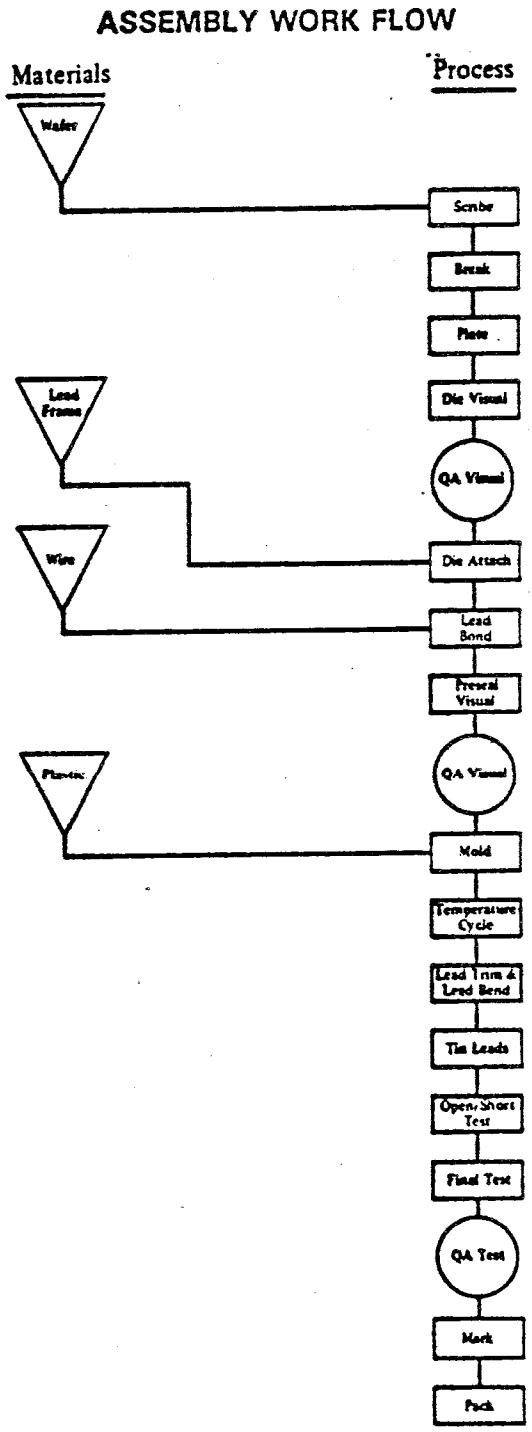
This consists of stamping identification information on the package.

I. Pack

Completed units are packed with static protective packaging and readied for shipment.

The flow of assembly can vary from company to company and this is only meant to be an outline covering major steps for purposes of the plant tour. Figure 5 shows a flow chart of assembly.

FIGURE 5


ASSEMBLY WORK FLOW
Materials
Process
Wafer
Lead Frame
Wire
Plastic
Scribe
Break
Plate
Die Visual
QA Visual
Die Attach
Lead Bond
Preseal Visual
QA Visual
Mold
Temperature Cycle
Lead Trim & Lead Bend
Tin Leads
Open/Short Test
Final Test
QA Test
Mark
Pack

VII. FINAL TEST

Final test is performed after the dice from the wafer have been put into packages. Each unit is tested across all worst case conditions. Devices are exercised for maximum and minimum speed, power and combinations of input/output.

Environmental conditions are guaranteed in one of two methods.

- Devices are tested at the high end of temperature specification, or
- Devices are tested at room temperature with wide enough tolerances so that operation at temperature is guaranteed (this is referred to as guardbanding).

At MOS Technology, a quality and reliability sample is taken from each batch of devices before shipment to a customer. This sample is subjected to a combined high temperature and operating voltage stress for several hours and must pass a subsequent test of operating characteristics before the batch is considered acceptable.

VIII. SUPPORT ACTIVITIES

A. Circuit Design

The function of this group is to take inputs from Marketing and customers and design the circuits needed to perform desired functions.

B. Product Engineering

The function of this group is to work with circuit design as the product is being conceived and designed. Product Engineers also aid Designers in writing test programs for wafer sort and final test. The Product Engineer also fully characterizes the circuits over full performance range.

C. Process Engineering

The function of this group is to develop and sustain the process for wafer fabrication.

D. Quality Assurance

The function of this group is to insure that documentation is maintained at each step of the manufacturing process. In addition, Quality Assurance must raise warning flags when "out-of-spec" conditions occur.

E. Equipment Maintenance

This group maintains the process and test equipment insuring that the manufacturing operation runs smoothly and efficiently.

F. Facilities Maintenance

This group is responsible for environmental control, purity of gases, chemicals for fab area, as well as disposal of all wastes.

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